**REMARKS**

Claims 1-25 are rejected in the present application. Claim 1 has been amended. No new matter has been added. The Applicants respectfully request reconsideration of the application in light of the amendments to the claims and the following remarks.

The Final Office Action objected to the drawings. Applicant is submitting herewith formal drawings in compliance with 37 C.F.R. 1.121(d).

The Final Office Action rejected claims 21 and 23-25 as anticipated by U.S. Patent No. 5,212,777 ("Gove").

The Final Office Action rejected claim 22 as obvious over Gove.

The Office Action rejected claims 1-20 as obvious over Gove in view of U.S. Patent No. 6,526,430 ("Hung").

**Interview Summary**

The Applicant notes with appreciation the telephonic interview with Examiner Li, the undersigned and co-inventor Paul Master conducted on September 8, 2009. The Applicant agrees with the Interview Summary Sheet provided at the end of the interview in which the Examiner indicated that she would consider written arguments as to heterogeneous computational elements and interconnections between the computational elements not being disclosed by Gove. The Examiner agreed that SIMD/MIMD art such as Gove probably did not anticipate the elements of the pending claims. Applicant agreed to review the specification and propose clarifying language as to the configuration of a group of computational elements to further distinguish Gove. The Examiner indicated that she would fully consider Applicant's arguments and response.

The claims generally relate to a system with two functional units of heterogeneous computational elements. As noted in the interview, the computational units are composed of heterogeneous computational elements that have different computational functions allowing greater flexibility and efficiency of different configurations. Further, the computational elements each allow computation of data and may be grouped with other computational elements to form a functional unit by changing connections between the elements themselves via an interconnection network. Finally, a first group of the heterogeneous computational elements is configurable to form a first functional unit to implement a first function through the interconnection network. A second group of the heterogeneous computational elements is configurable to form a second functional unit to implement a second function through the interconnection network. If the second function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by forming one or more additional instances of the first functional unit. The reconfiguration of the second group of heterogeneous computational elements may take place while the first group of computational elements is performing the first function thus providing on the fly flexibility for an adaptable hardware device as explained in paragraphs 11-12 of the specification.

The adaptable device has a plurality of heterogeneous computational elements and an interconnection network is coupled to the plurality of heterogeneous computational elements such as computational elements 250A-D as shown in Fig. 3 and explained by paragraph 39 and 46. Such elements are configurable by the network 210 in response to configuration information that changes the interconnections between the elements as explained by paragraph 40-41 and 47. The differences between an adaptable device having homogeneous or identical computational elements (e.g., FPGAs) and having heterogeneous computational elements (the claims) is

detailed in paragraphs 6, 7, 15, 35, 39, 66 of the specification. Another specific example of different computational units with heterogeneous computational elements is shown in Fig. 4 and explained in paragraph 51.

Computational elements are fixed architecture elements that have different functions such as addition, multiplication, complex multiplication and subtraction. (paragraph 15) Such computational elements differ from other fixed circuit elements such as memory in their performance of a data function. Further different groups of computational elements may be interconnected using the interconnection network to cooperate to perform different functions. Examples of different configurations using different groups of computational elements are shown in Figs. 5A-5E and explained further in paragraphs 56-61 of the specification.

Gove relates to a multi-processor system that may be operated in single instruction multiple data (SIMD) and multiple instruction multiple data modes (MIMD). As explained at Col. 6, ll. 6-22, the reconfiguration of modes does not involve changing interconnections between the hardware, it is instead changing the pre-determined modes of the processors. Gove is still software based and relies on the "reconfiguration" based on different modes of individual processor operation since it only changes the connections so processors may access different memory devices. As discussed Gove does not disclose hardware reconfiguration based on changing interconnections between computational elements. Further Gove does not disclose different computational units having different types of computational elements (heterogeneous). All of the examples cited by the Final Office Action such in Fig. 10, all show a single unit having multiple identical processors (PP1, PP2, etc.) that are coupled together and therefore connections cannot be changed between such elements to form additional units to perform a function. The Final Office Action has cited Col. 9, l. 27-Col. 10, l. 4 and Fig. 10, but this section

only relates to the use of a crossbar switch 20 to connect the processors to different memories. The processors themselves are not reconfigured, they are simply switched between single and multiple instruction modes by coupling them to different memories.

Hung relates to a dual processor system having a normal generic processor core 110 and a software reconfigurable co-processor 140. The software reconfigurable co-processor appears to have a number of pre-prepared functions that may be selected via software. Neither of the processors in Hung relate to hardware configuration of either processor. Hung therefore is fundamentally different from hardware reconfiguration since the so-called configuration in Hung is actually performed by software.

Claims 1, 6, 11, 16 and 21 require a computational units or matrices having heterogeneous computational elements. As explained above, Gove does not disclose two computational units with a plurality of heterogeneous computational elements as all of the processors, P0-Pn, are identical.

Second, these claims require reconfiguration by changing the connections between the computational elements via the interconnection networks. As explained above, Gove only discloses changing connections between the memory elements and the computational elements (processors). The connection between the processors P0-Pn, (processor bus 40) stays fixed as shown in Fig. 4 of Gove.

Finally, these claims require the configuration of groups of computational elements to perform a first function and the configuration of another group of computational elements to perform a second function, and if the second function is no longer needed, the reconfiguration of the computational elements to a first function. The Final Office Action has cited Col. 9, l. 5 to Col 10, l. 5 of Hung as teaching reconfiguration of computational elements based on need and

availability. However, the section cited by the Examiner does not have any suggestion to reconfigure elements formally performing a second function during the operation of other computational elements performing a first function. This section describes the performance of the single co-processor 140 of different functions A, B and C via programming which is not hardware reconfiguration via switching interconnections between multiple computational elements. (Col. 9, ll. 5-33). Further, this section assumes that the entirety of the processor is switched to the performance of a different give function. In contrast, these claims require that the second heterogeneous computational unit or units are reconfigurable while the first functional unit implements the first operating mode. Neither Gove nor Hung discloses reconfiguration of parts of the computational unit while the first function is being performed. Both Gove and Hung require configuration and reconfiguration as the entirety of the computational unit to take place before the operation of the adaptive circuit.

Applicant respectfully submits that Gove does not disclose groups of computational elements that are configured into functional units as defined by the claims. The processors in Gove are not grouped together via an interconnection network to perform a function. In order to further differentiate Gove, Applicant has amended claim 1 to require that "a first functional unit is configured by establishing connections between a first group of the first and second plurality of heterogeneous computational elements via the interconnection networks to implement a first function" and similarly a second functional unit is configured by establishing connections between a second group of heterogeneous computational elements. Gove does not disclose these elements because each processor in Gove behaves independently and Gove does not disclose combining processors via changing connections between them to create a functional unit using the processors to jointly perform a function. Further, the processors in Gove are not combined

with other processors via interconnections to perform different functions since the connections between the processors remain constant.

**CONCLUSION**

In view of the above amendments and remarks, the Applicants believe that all of the claims are in condition for allowance and action towards that effect is respectfully requested. If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is requested to contact the undersigned attorney at the number indicated. It is believed that no additional fees are due in connection with this Amendment and Response.

However, in the event that any additional fees are required (except for payment of the issue fee), the Commissioner is authorized to deduct the fees.

Respectfully submitted,

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/Wayne L. Tang/

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